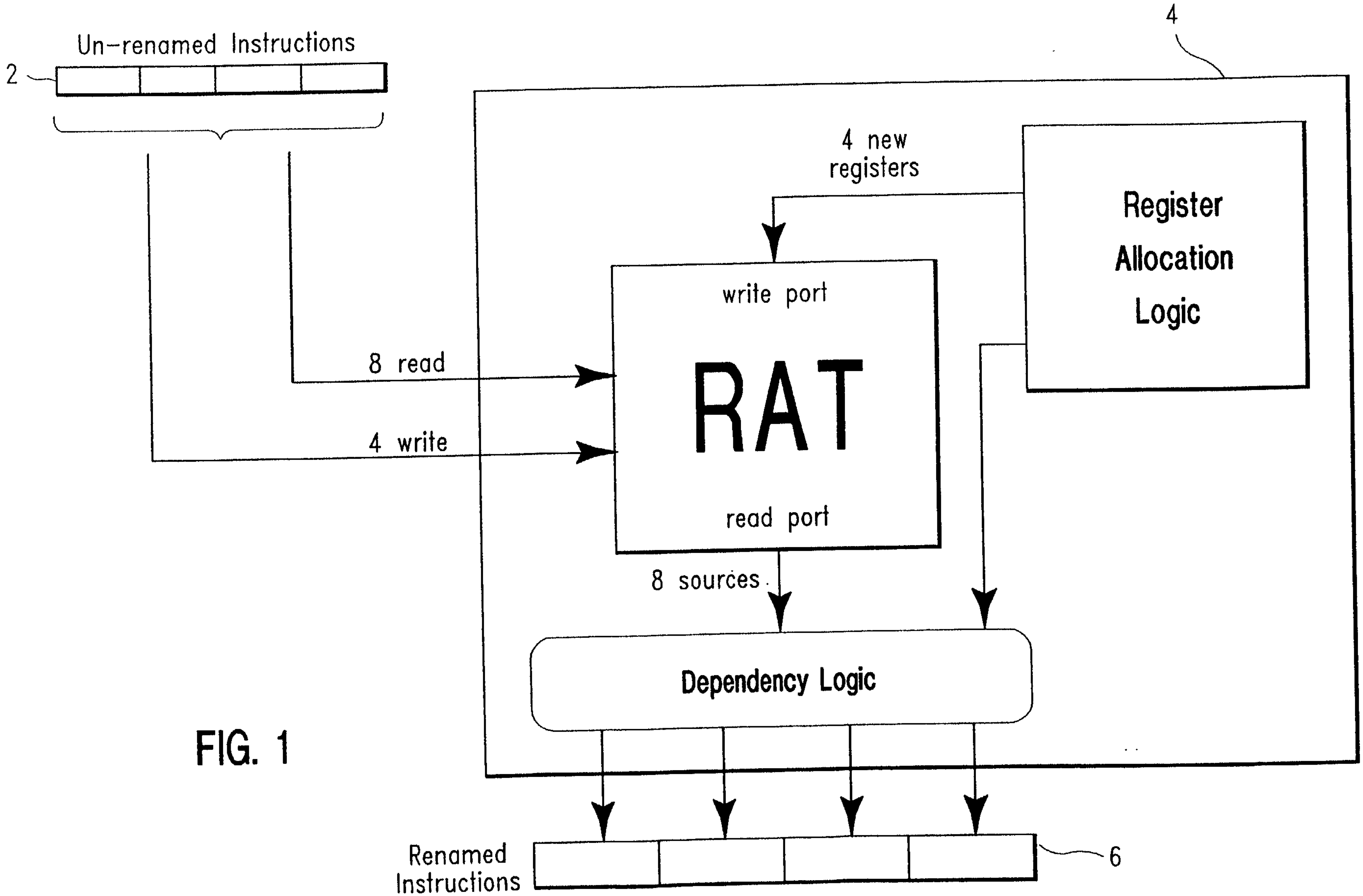
Un-renamed Instructions
2
4
4 new
registers
Register
Allocation
Logic
write port
RAT
read port
8 read
4 write
8 sources
Dependency Logic
Renamed
Instructions
6

FIG. 1

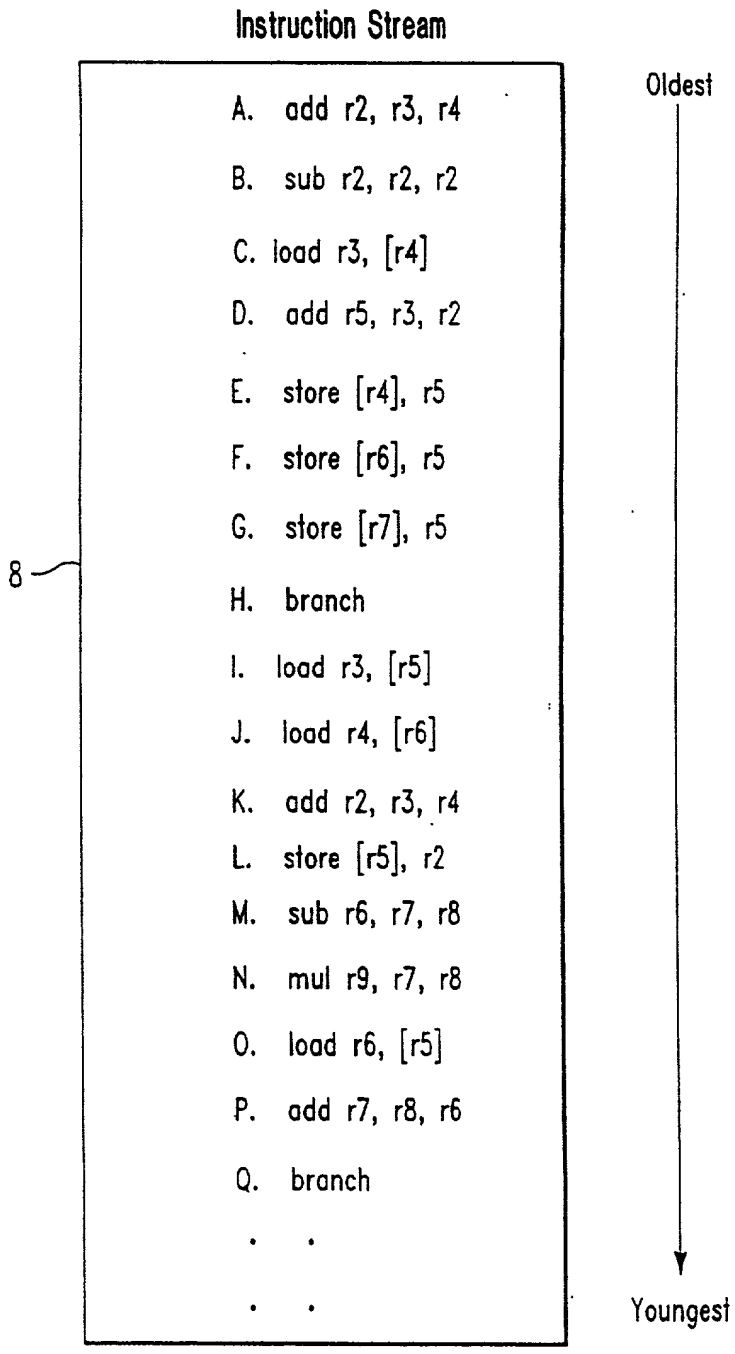

FIG. 2

Instructions Packetized in Trace Cache

A	B	C	D	E	F	G	H	10
I	J	K	L	M				12
N	O	P	Q	...	...			14

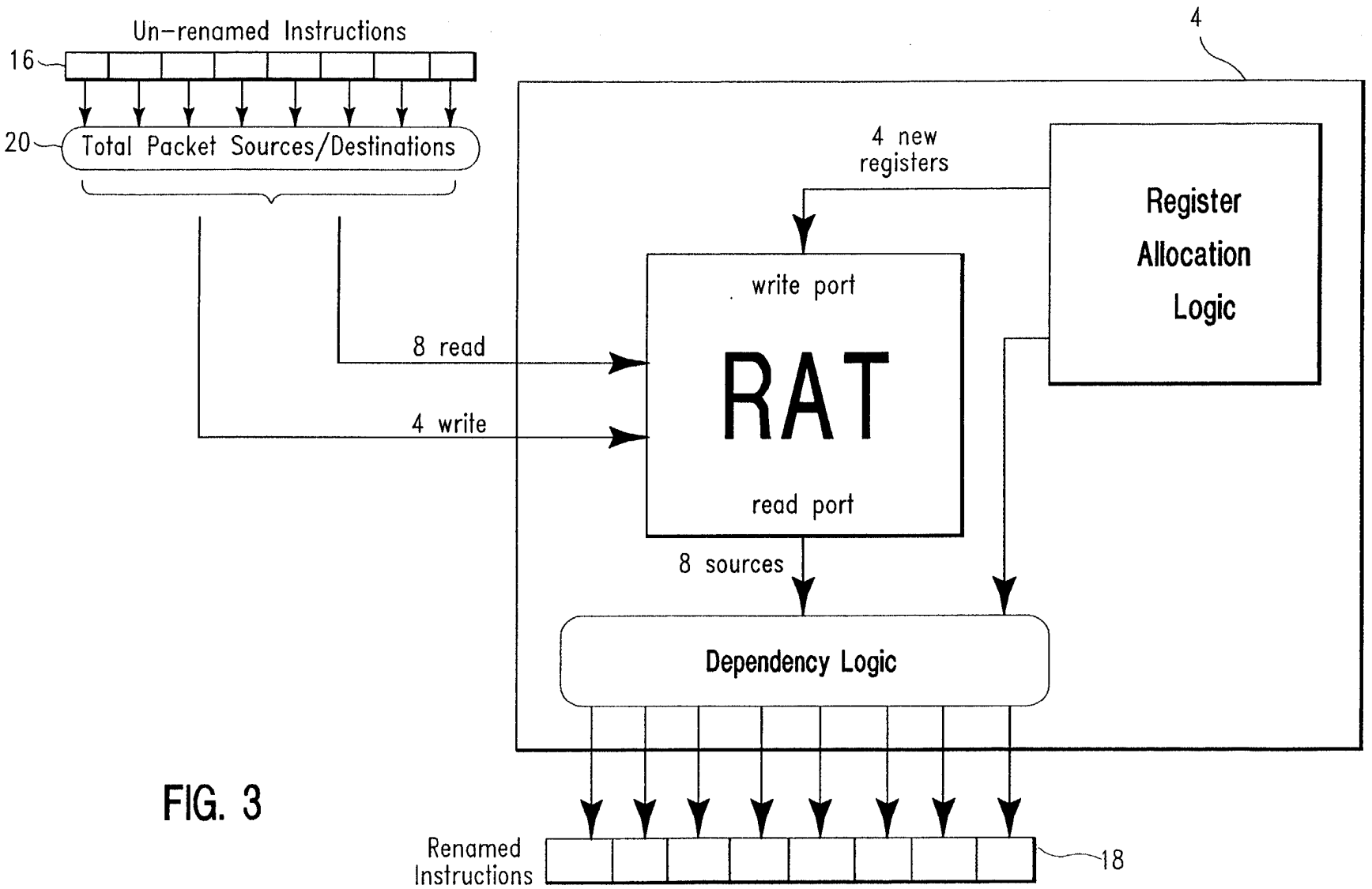
Un-renamed Instructions
16
20
Total Packet Sources/Destinations
4
4 new registers
Register Allocation Logic
write port
RAT
read port
8 read
4 write
8 sources
Dependency Logic
Renamed Instructions
18

FIG. 3